In the Claims:

1. (Previously Amended) An apparatus for detecting a correlation of samples with a spread code, said samples being obtained by sampling a spectrum spread signal in a range of one symbol period with a oversampling rate which is N-fold of a chip rate, wherein N is an integer larger than zero, said spread code being of L × M period per symbol, wherein L and M are integers larger than one, said spectrum spread signal having been spread in spectrum by said spread code signal, said apparatus comprising:

an L-chip accumulator which inputs said samples to generate and output an intermediate correlation signal;

M memories, each of which stores L x M samples of said intermediate correlation signal;

an adder which has M input terminals and inputs from each of said input terminals one of said intermediate correlation signal which is outputted from said L-chip accumulator and said intermediate correlation signal which is outputted from a corresponding memory among said memories; and

a controller which supplies said intermediate correlation signal outputted from said L-chip accumulator to said M memories and to said M input terminals of said adder in rotation with a unit of L × N samples, and reads, and supplies to each of said input terminals of said adder, said intermediate correlation signal which has been stored in each of said memories M-1 times;

wherein an output of said adder is outputted as an correlation signal outputted from the apparatus.

2. (Previously Amended) The apparatus according to claim 1, further comprising:

M multipliers, each of which is connected with each of said memories and with each ~~of said input terminals of said adder~~; and

a coefficient generator which generates coefficients of said multipliers;

wherein each of said coefficients changes cyclically in a unit of L × N-fold of a period corresponding to said oversampling rate.

3. (Original) The apparatus according to claim 1, wherein said memories are one-port type of memories.

4. (Original) The apparatus according to claim 1, wherein said L-chip accumulator is a matching filter.

5. (Original) The apparatus according to claim 1, wherein said L-chip accumulator is a correlator bank.

6. (Currently Amended) An apparatus for detecting a correlation, comprising:

an accumulator which inputs a reception signal to output a first correlation signal in response to said reception signal, said first correlation signal including first data and second data following to said first data;

a first memory which stores said first data included in said first correlation signal;

a second memory which stores said second data included in said first correlation signal; and

an adder;

wherein said first data is supplied to said adder in a first period when said first data are written to said first memory;

wherein ~~said second data and~~ said second data , and said first data which have been stored in said first ~~memory are~~ memory, are supplied to said adder in a second period when said second data are written to said second memory; and

wherein an output of said adder is outputted as a final correlation signal.

7. (Previously Amended) An apparatus for detecting correlation, comprising:

an accumulator which outputs a first correlation signal in response to a reception signal;

a plurality of memories, each of said memories stores said first correlation signal in a respective prescribed period;

an adder which inputs said first correlation signals from said plurality of memories and from said accumulator; and

a controller which supplies to said adder said first correlation signals which have been stored in memories other than a first memory among said plurality of memories when said first correlation signal is written to said first memory.

8. (Original) A spectrum despread apparatus comprising the apparatus according to claim 1.

9. (Original) A spectrum despread apparatus comprising the apparatus according to claim 6.

10. (Original) A spectrum despread apparatus comprising the apparatus according to claim 7.

11. (Original) A reception terminal comprising the apparatus according to claim 1.

12. (Original) A reception terminal comprising the apparatus according to claim 6.

13. (Original) A reception terminal comprising the apparatus according to claim 7.

14. (Original) A transmission/reception terminal comprising the apparatus according to claim 1.

15. (Original) A transmission/reception terminal comprising the apparatus according to claim 6.

16. (Original) A transmission/reception terminal comprising the apparatus according to claim 7.

17. (Currently Amended) A method for detecting a correlation of samples with a spread code, said samples being obtained by sampling a spectrum spread signal in a range of one symbol period with a oversampling rate which is N-fold of a chip rate, wherein N is an integer larger than zero, said spread code being of L × M period per symbol, wherein L and M are integers larger than one, said spectrum spread signal having been spread in spectrum by said spread code signal, said method comprising steps of:

generating an intermediate correlation signal by using said samples;

writing samples of said intermediate correlation signal to M memories in rotation with a unit of L × N samples;

supplying the samples of said intermediate correlation signal to M input terminals of an adder simultaneously with the step of writing;

reading L x M samples of said intermediate correlation signal which have been stored in each of said ~~memories M-1 times~~ memories M-1 times;

supplying the samples read in the step of reading to each of said input terminals of said adder; and

outputting an output of said adder as a correlation signal.

18. (Original) The method according to claim 17, further comprising a step of multiplying the samples supplied to each of input terminals of said adder with a coefficient which changes cyclically in a unit of L × N-fold of a period corresponding to said oversampling rate.